



## Silicon Anomaly

## ADuC7033

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7033 integrated precision battery sensor. The anomalies listed apply to all ADuC7033 packaged material branded as follows:

First Line ADuC7033  
Second Line BSTZ 8L or BCPZ 8L

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

### ADuC7033 FUNCTIONALITY ISSUES

| Silicon Revision Identifier | Kernel Revision Identifier | Chip Marking                   | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|-----------------------------|----------------------------|--------------------------------|----------------|---------------|---------------------------|
| 8L                          | A60                        | ADuC7033<br>BSTZ 8L or BCPZ 8L | Release        | Rev. A        | 3                         |

### ADuC7033 PERFORMANCE ISSUES

| Silicon Revision Identifier | Kernel Revision Identifier | Chip Marking                   | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|-----------------------------|----------------------------|--------------------------------|----------------|---------------|---------------------------|
| 8L                          | A60                        | ADuC7033<br>BSTZ 8L or BCPZ 8L | Release        | Rev. A        | 2                         |

#### Rev. A

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## ANOMALIES

## ADuC7033 Functionality Issues

## 1. LIN Communication with VDD &gt; 31 V [er001]:

|                        |                                                                       |
|------------------------|-----------------------------------------------------------------------|
| <b>Background:</b>     | The ADuC7033 is specified for operation up to 40 V.                   |
| <b>Issue:</b>          | If the LIN communication occurs with VDD > 31 V, the ADuC7033 resets. |
| <b>Workaround:</b>     | Pending.                                                              |
| <b>Related Issues:</b> | None.                                                                 |

## 2. LIN Short-Circuit Recognition [er002]:

|                        |                                                                                                                                                                                                                   |
|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Background:</b>     | The ADuC7033 features LIN short-circuit protection. In the event of a short circuit on the LIN bus, an interrupt is generated. HVCFG1[2] allows users to enable/disable this interrupt. It is enabled by default. |
| <b>Issue:</b>          | If the LIN is shorted to VDD with a resistance lower than 120 $\Omega$ , LIN can oscillate over temperature and supply and a short may not be detected.                                                           |
| <b>Workaround:</b>     | Pending.                                                                                                                                                                                                          |
| <b>Related Issues:</b> | None.                                                                                                                                                                                                             |

## 3. Power-On Reset [er003]:

|                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Background:</b> | The ADuC7033 integrates a power-on reset (POR) circuit holding the ASIC in reset for 20 ms typically after VDD reaches 3 V typically.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Issue:</b>      | Under particular conditions, the POR does not release the reset signal, that is, the ASIC remains in reset until a power cycle occurs. This POR issue only occurs under three specific and coincident power-on conditions: <ul style="list-style-type: none"> <li>• Fast ramp on VDD, nominally faster than 100 <math>\mu</math>s from <math>V_{init}</math> to 12 V</li> <li>• Initial value of VDD (<math>V_{init}</math>) <math>\sim</math>1.2 V</li> <li>• Voltage on REG_DVDD at time the VDD ramp is reapplied <math>\sim</math>175 mV</li> </ul>                                                                                                                                                                         |
| <b>Workaround:</b> | A fast VDD ramp (that is, ramping from $\sim$ 1.2 V to 12 V in $<$ 100 $\mu$ s) is required as one of the conditions to initiate the reported POR issue. Analog Devices recommends careful selection of external power supply decoupling components to ensure that the VDD supply ramp rate can always be guaranteed to be $>$ 100 $\mu$ s under all VBAT power-on conditions. Specifically, in modules that already incorporate a series resistor and decoupling capacitor to ground on the VDD line between the reverse protection diode and the VDD pin (see Figure 1), choose the series resistor/decoupling capacitor combination to give an RC time constant of at least 100 $\mu$ s, such as 10 $\Omega$ and 10 $\mu$ F. |

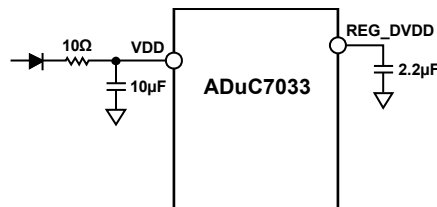


Figure 1.

Alternatively, in the specific case of customer modules where the VDD decoupling capacitor cannot be increased beyond 4.7  $\mu$ F, then increasing the series resistor to 20  $\Omega$  and increasing the REG\_DVDD decoupling capacitor from 2.2  $\mu$ F to 10  $\mu$ F also slews the VDD supply power-on ramp to  $\sim$ 200  $\mu$ s. This is also an appropriate and recommended containment measure.

|                        |       |
|------------------------|-------|
| <b>Related Issues:</b> | None. |
|------------------------|-------|

**ANOMALIES****ADuC7033 Performance Issues****1. ESD [pr001]:**

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|                        |                                                                                                                          |
|------------------------|--------------------------------------------------------------------------------------------------------------------------|
| <b>Background:</b>     | The ADuC7033 is intended to be classified for HBM ESD rating of 2 kV and FICDM ESD rating of 500 V.                      |
| <b>Issue:</b>          | For silicon branded 8L, HBM ESD is specified to 800 V and FICDM ESD is specified to 400 V and 750 V for the corner pins. |
| <b>Workaround:</b>     | Pending.                                                                                                                 |
| <b>Related Issues:</b> | None.                                                                                                                    |

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**2. WU Pin Latch-Up [pr002]:**

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|                    |                                                                                                                                 |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------|
| <b>Background:</b> | The latch-up condition on the WU pin should follow the AECQ100 specification and should be able to sink up to -100 mA at 125°C. |
| <b>Issue:</b>      | The WU pin fails the AECQ100 specification.                                                                                     |
| <b>Workaround:</b> | It is recommended to use a protection diode such as a BAS52, as shown in Figure 2, to avoid destructive damage to the part.     |

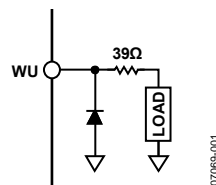


Figure 2. Protection Diode on WU Pin

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|                        |       |
|------------------------|-------|
| <b>Related Issues:</b> | None. |
|------------------------|-------|

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**SECTION 1. ADuC7033 FUNCTIONALITY ISSUES**

| Reference Number | Description                       | Status |
|------------------|-----------------------------------|--------|
| er001            | LIN communication with VDD > 31 V | Open   |
| er002            | LIN short-circuit recognition     | Open   |
| er003            | Power-on reset                    | Open   |

**SECTION 2. ADuC7033 PERFORMANCE ISSUES**

| Reference Number | Description     | Status |
|------------------|-----------------|--------|
| pr001            | ESD             | Open   |
| pr002            | WU pin latch-up | Open   |